AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions, and listings, of claims in the application:

1. (Amended) ~~An integrated~~ A circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first PMOS device and a first NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

mode control circuit transistors that serve as power and power ground source transistors when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistors when the multi-state circuit is in the standby mode, including,

a second NMOS device, with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; and

a second PMOS device, with a drain connected to an effective ground terminal and with a source connected to a source of the first NMOS device[[.]] ;

wherein the multi-state circuit and the mode control circuit transistors are disposed in an integrated circuit;

means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode; and

means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode.

2. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the second NMOS device is a **depletion** transistor; and

the second PMOS device is a **depletion** transistor.

3. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the first PMOS device is an **ordinary enhancement** transistor;

the first NMOS device is an **ordinary enhancement** transistor;

the second NMOS device is a **depletion** transistor; and

the second PMOS device is a **depletion** transistor.

4. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the first PMOS device is a low threshold voltage **ordinary enhancement** transistor;

the first NMOS device is a low threshold voltage **ordinary enhancement** transistor;

the second NMOS device is a **depletion** transistor; and

the second PMOS device is a **depletion** transistor.

5. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the second NMOS device is a **leaky enhancement** transistor; and

the second PMOS device is a **leaky enhancement** transistor.

6. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the first PMOS device is an **ordinary enhancement** transistor;

the first NMOS device is an **ordinary enhancement** transistor;

the second NMOS device is a **leaky enhancement** transistor; and

the second PMOS device is a **leaky enhancement** transistor.

7. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the first PMOS device is a low threshold voltage **ordinary enhancement** transistor;

the first NMOS device is a low threshold voltage **ordinary enhancement** transistor;

the second NMOS device is a **leaky enhancement** transistor; and

the second PMOS device is a **leaky enhancement** transistor.

8. (Amended) The ~~integrated~~ circuit of claim 1 further including:

a first logic input to a gate of the first PMOS device; and

a second logic input to a gate of the first NMOS device.

9. (Amended) The ~~integrated~~ circuit of claim 1 further including:

a logic input to a gate of the first PMOS device and to a gate of the first NMOS device.

10. (Amended) The ~~integrated~~ circuit of claim 1 further including:

a first logic input to a gate of the first PMOS device;

a second logic input to a gate of the first NMOS device;

a first control input to a gate of the second NMOS device; and

a first control input to a gate of the second PMOS device.

11. (Amended) The ~~integrated~~ circuit of claim 1 further including:

at least one control input to the multi-state circuit connected to control the state of the multi-state circuit when the second NMOS device and the second PMOS device are turned on;

respective control inputs to the respective second NMOS device and to the second PMOS device connected to control turn on and turn off of the second NMOS device and the second PMOS device so as to turn them on together and to turn them off together;

whereby the at least one control input to the multi-state circuit does not effect changes in state of the multi-state circuit when the second NMOS device and the second PMOS device are turned off.

12. (Amended) The ~~integrated~~ circuit of claim 1 further including:

a pull-up sustaining NMOS device with a with a drain connected to the supply voltage terminal and with a source connected to a source of the first PMOS device and with a gate connected to an output node of the multi-state circuit; and

a pull-down sustaining PMOS device with a with a drain connected to the effective ground terminal and with a source connected to the source of the first NMOS device and with a gate connected to the output node of the multi-state circuit.

13. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the first PMOS device and the second NMOS device are sized relative to each other so that a channel conduction of the second NMOS device is sufficiently less than that of the first PMOS device such that, when the multi-state circuit is in the active mode, the second NMOS device becomes reverse biased when the multi-state circuit is in the second state and second NMOS device is turned off. ~~(IS THIS CLAIM OK?)~~

14. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the first NMOS device and the second PMOS device are sized relative to each other so that a channel conduction of the second PMOS device is sufficiently less than that of the first NMOS device such that, when the multi-state circuit is in the active mode, the second PMOS device becomes reverse biased when the multi-state circuit is in the first state and second PMOS device is turned off. ~~(IS THIS CLAIM OK?)~~

15. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the first PMOS device and the second NMOS device are sized relative to each other so that a channel conduction of the second NMOS device is sufficiently less than that of the first PMOS device such that, when the multi-state circuit is in the active mode, the second NMOS device becomes reverse biased when the multi-state circuit is in the second state and second NMOS device is turned off; and

the first NMOS device and the second PMOS device are sized relative to each other so that a channel conduction of the second PMOS device is sufficiently less than that of the first NMOS device such that, when the multi-state circuit is in the active mode, the second PMOS device becomes reverse biased when the multi-state circuit is in the first state and second PMOS device is turned off. ~~(IS THIS CLAIM OK?~~

16. (Amended) The ~~integrated~~ circuit of claim 1 wherein,

the multi-state circuit includes multiple first PMOS devices, and further including;

one or more second NMOS device having a source connected to respective sources of one or more of the multiple first PMOS devices.

17. (Amended) ~~An integrated~~ A circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first **ordinary enhancement** PMOS device and a first **ordinary enhancement** NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

mode control circuit transistors that serve as power and power ground source transistors when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistors when the multi-state circuit is in the standby mode, including,

a second **depletion or leaky enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; and

a second **depletion or leaky enhancement** PMOS device with a drain connected to a an effective ground terminal and with a source connected to a source of the first NMOS device;

wherein the first PMOS device and the second NMOS device are sized relative to each other so that a channel conduction of the second NMOS device is sufficiently less than that of the first PMOS device such that, when the multi-state circuit is in an active mode, the second NMOS device becomes reverse biased when the multi-state circuit is in the second state and second NMOS device is turned off; and

wherein the first NMOS device and the second PMOS device are sized relative to each other so that a channel conduction of the second PMOS device is sufficiently less than that of the first NMOS device such that, when the multi-state circuit is in an active mode, the second PMOS device becomes reverse biased when the multi-state circuit is in the first state and second PMOS device is turned off[[.]] ;

wherein the multi-state circuit and the mode control circuit transistors are disposed in an integrated circuit;

means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode; and

means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode.

18. (Amended) The ~~integrated~~ circuit of claim 17 further including:

a pull-up sustaining **depletion or leaky enhancement** NMOS device with a with a drain connected to the supply voltage terminal and with a source connected to a source of the first PMOS device and with a gate connected to an output node of the multi-state circuit; and

a pull-down sustaining **depletion or leaky enhancement** PMOS device with a with a drain connected to the effective ground terminal and with a source connected to the source of the first NMOS device and with a gate connected to the output node of the multi-state circuit.

19. (Amended) ~~An integrated~~ A circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first **ordinary enhancement** PMOS device and a first **ordinary enhancement** NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

mode control circuit transistors that serve as power and power ground source transistors when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistors when the multi-state circuit is in the standby mode, including,

a second **ordinary enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; and

a second **ordinary enhancement** PMOS device with a drain connected to a an effective ground terminal and with a source connected to a source of the first NMOS device;

wherein the first PMOS device and the second NMOS device are sized relative to each other so that a channel conduction of the second NMOS device is sufficiently less than that of the first PMOS device such that, when the multi-state circuit is in an active mode, the second NMOS device becomes reverse biased when the multi-state circuit is in the second state and second NMOS device is turned off; [[and]]

wherein the first NMOS device and the second PMOS device are sized relative to each other so that a channel conduction of the second PMOS device is sufficiently less than that of the first NMOS device such that, when the multi-state circuit is in an active mode, the second PMOS device becomes reverse biased when the multi-state circuit is in the first state and second PMOS device is turned off[[.]] ;

wherein the multi-state circuit and the mode control circuit transistors are disposed in an integrated circuit;

means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode; and

means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode.

20. (Amended) The ~~integrated~~ circuit of claims 19 further including:

a pull-up sustaining **ordinary enhancement** NMOS device with a with a drain connected to the supply voltage terminal and with a source connected to a source of the first PMOS device and with a gate connected to an output node of the multi-state circuit; and

a pull-down sustaining **ordinary enhancement** PMOS device with a with a drain connected to the effective ground terminal and with a source connected to the source of the first NMOS device and with a gate connected to the output node of the multi-state circuit.

21. (Amended) ~~An integrated~~ A circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first PMOS device and a first NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

mode control circuit transistors that serve as power and power ground source transistors when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistors when the multi-state circuit is in the standby mode, including,

a second **ordinary enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; [[and]]

a second **ordinary enhancement** PMOS device with a drain connected to a an effective ground terminal and with a source connected to a source of the first NMOS device[[.]] ;

wherein the multi-state circuit and the mode control circuit transistors are disposed in an integrated circuit;

means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode; and

means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode.

22. (Amended) ~~An integrated~~ A circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first **ordinary enhancement** PMOS device and a first **ordinary enhancement** NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

mode control circuit transistors that serve as power and power ground source transistors when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistors when the multi-state circuit is in the standby mode, including,

a second **ordinary enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; [[and]]

a second **ordinary enhancement** PMOS device with a drain connected to a an effective ground terminal and with a source connected to a source of the first NMOS device[[.]] ;

wherein the multi-state circuit and the mode control circuit transistors are disposed in an integrated circuit;

means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode; and

means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode.

23. (Amended) ~~An integrated~~ A circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first **low threshold ordinary enhancement** PMOS device and a first **low threshold ordinary enhancement** NMOS device, the multi-state circuit

being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

mode control circuit transistors that serve as power and power ground source transistors when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistors when the multi-state circuit is in the standby mode, including,

a second **ordinary enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; [[and]]

a second **ordinary enhancement** PMOS device with a drain connected to a an effective ground terminal and with a source connected to a source of the first NMOS device[[.]] ;

wherein the multi-state circuit and the mode control circuit transistors are disposed in an integrated circuit;

means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode; and

means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode.

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Amended) ~~An integrated~~ A circuit for use with a supply voltage and an effective ground voltage comprising:

a ~~an enhancement~~ NMOS transistor with a drain connected to a supply voltage terminal; and

a multi-state circuit connected to a source of the NMOS transistor and connected to an effective ground terminal[[.]] ;

wherein the NMOS transistor operates as a power source transistor when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistor when the multi-state circuit is in the standby mode; and

wherein the NMOS transistor and the multi-state circuit are disposed in an integrated circuit;

means for providing a turn on voltage signal to a gate of the NMOS transistor that is higher than the supply voltage when the multi-state circuit is in an active mode

30. (Amended) ~~An integrated~~ A circuit for use with a supply voltage and an effective ground voltage comprising:

a ~~an enhancement~~ PMOS transistor with a drain connected to an effective ground voltage terminal; [[and]]

a multi-state circuit connected to a supply voltage terminal and connected to a source of the PMOS transistor[[.]] ;

wherein the PMOS transistor operates as a power ground source transistor when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistor when the multi-state circuit is in the standby mode; and

wherein the PMOS transistor and the multi-state circuit are disposed in an integrated circuit;

means for providing a turn on voltage signal to a gate of the PMOS transistor that is lower than the effective ground voltage when the multi-state circuit is in an active mode.

31. (Amended) ~~An integrated~~ A circuit for use with a supply voltage and an effective ground voltage comprising:

a ~~an enhancement~~ NMOS transistor with a drain connected to a supply voltage terminal;

a ~~an enhancement~~ PMOS transistor with a drain connected to an effective ground voltage terminal; [[and]]

a multi-state circuit connected to a source of the NMOS transistor and connected to source of the PMOS transistor[[.]] ;

wherein the NMOS transistor operates as a power source transistor when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistor when the multi-state circuit is in the standby mode;

wherein the PMOS transistor operates as a power ground source transistor when the multi-state circuit is in an active mode and that serve as self-reverse biased cut-off transistor when the multi-state circuit is in the standby mode;

wherein the NMOS transistor, the PMOS transistor and the multi-state circuit are disposed in an integrated circuit;

means for providing a turn on voltage signal to a gate of the NMOS transistor that is higher than the supply voltage when the multi-state circuit is in an active mode; and

means for providing a turn on voltage signal to a gate of the PMOS transistor that is lower than the effective ground voltage when the multi-state circuit is in an active mode.

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (New) The circuit of claim 1, 17, 19, 21, 22, 23 or 31,

wherein the means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode includes an on-chip voltage generator disposed in the integrated circuit; and

wherein the means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode includes an on-chip voltage generator disposed in the integrated circuit.

36. (New) The circuit of claim 1, 17, 19, 21, 22, 23 or 31,

wherein the means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode includes an off-chip voltage generator disposed off the integrated circuit; and

wherein the means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode includes an off-chip voltage generator disposed off the integrated circuit.

37. (New) The circuit of claim 29,

wherein the means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode includes an on-chip voltage generator disposed in the integrated circuit; and

38. (New) The circuit of claim 29,

wherein the means for providing a turn on voltage signal to a gate of the second NMOS device that is higher than the supply voltage when the multi-state circuit is in an active mode includes an off-chip voltage generator disposed off the integrated circuit; and

39. (New) The circuit of claim 30,

wherein the means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode includes an on-chip voltage generator disposed in the integrated circuit.

40. (New) The circuit of claim 30,

wherein the means for providing a turn on voltage signal to a gate of the second PMOS device that is lower than the effective ground voltage when the multi-state circuit is in an active mode includes an off-chip voltage generator disposed off the integrated circuit.